# Laboratory Report # 1

**Name:** Machacon, Zach Riane I. **Date Completed:** September 1, 2023

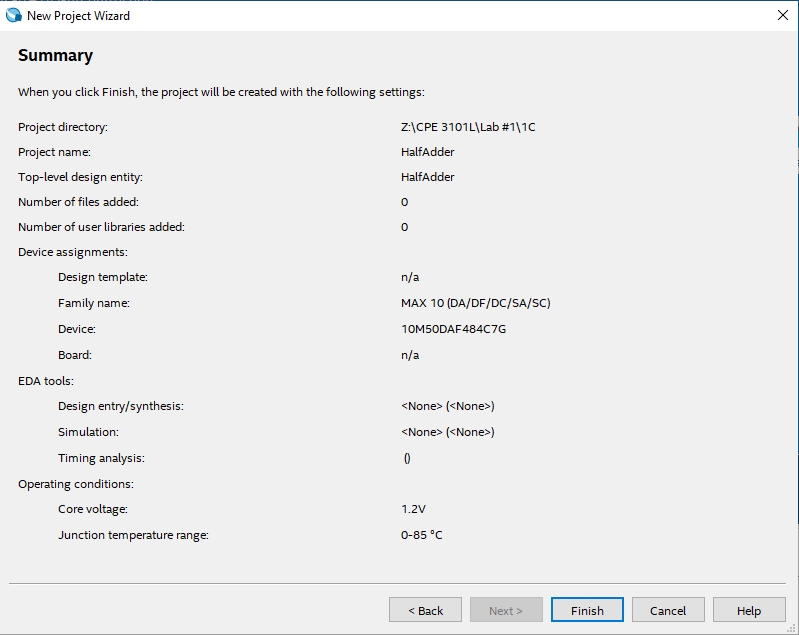
**Laboratory Exercise Title:** Design Flow of Digital Systems

***Target Course Outcomes:***

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

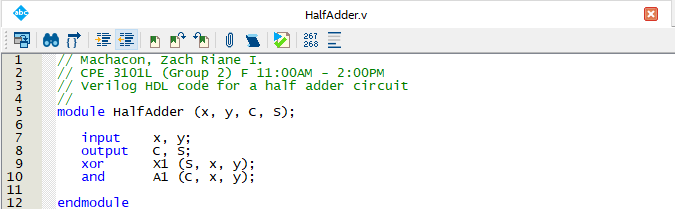
**CO2:** Verify the functionality of HDL-based components through design verification tools.

**Exercise 1C:**

**

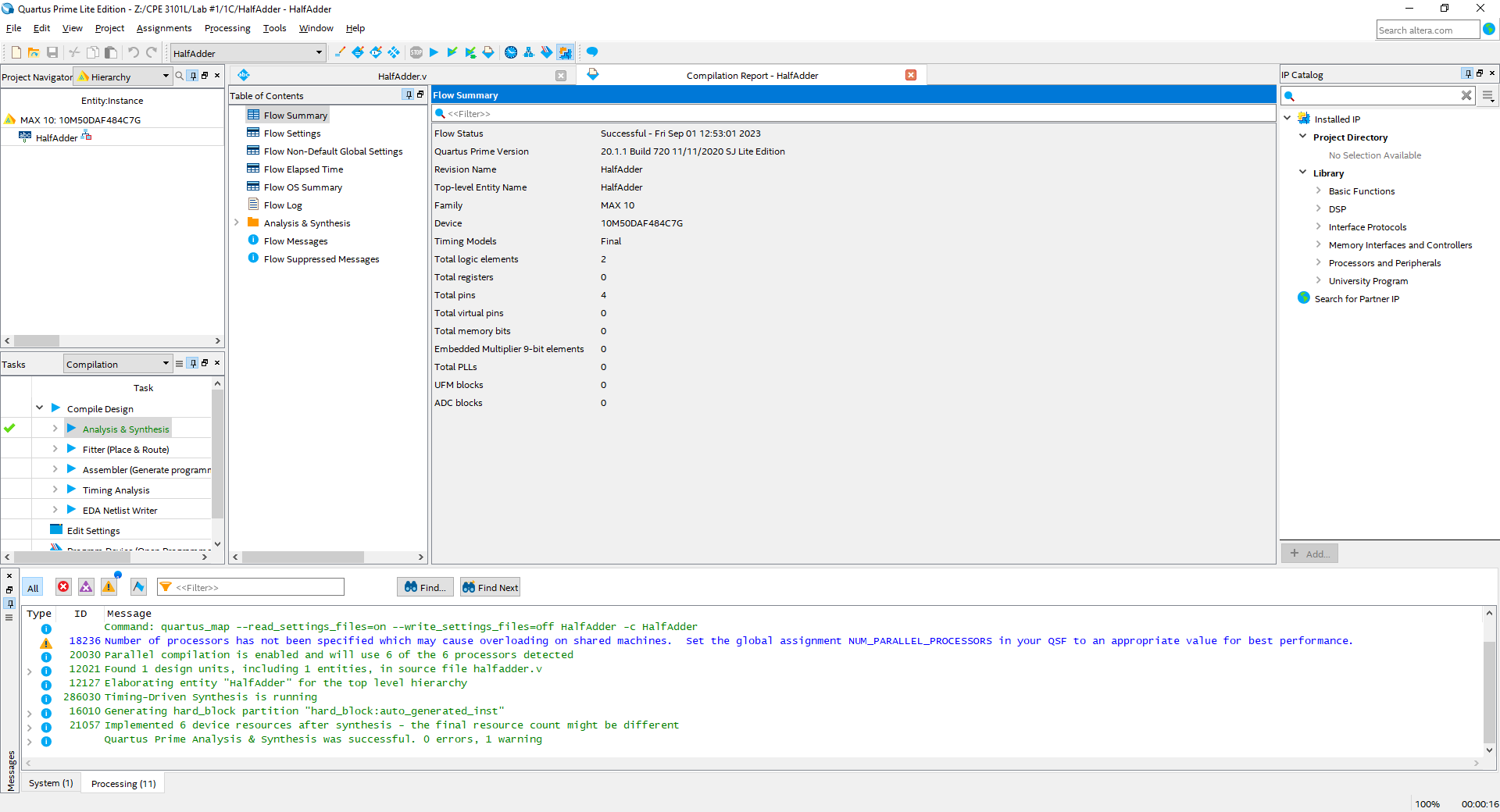
**Figure 1: Project Settings Summary of HalfAdder**

The project made use of DE-10 Lite board with an Intel Max 10 10M50DAF484C7G FPGA.



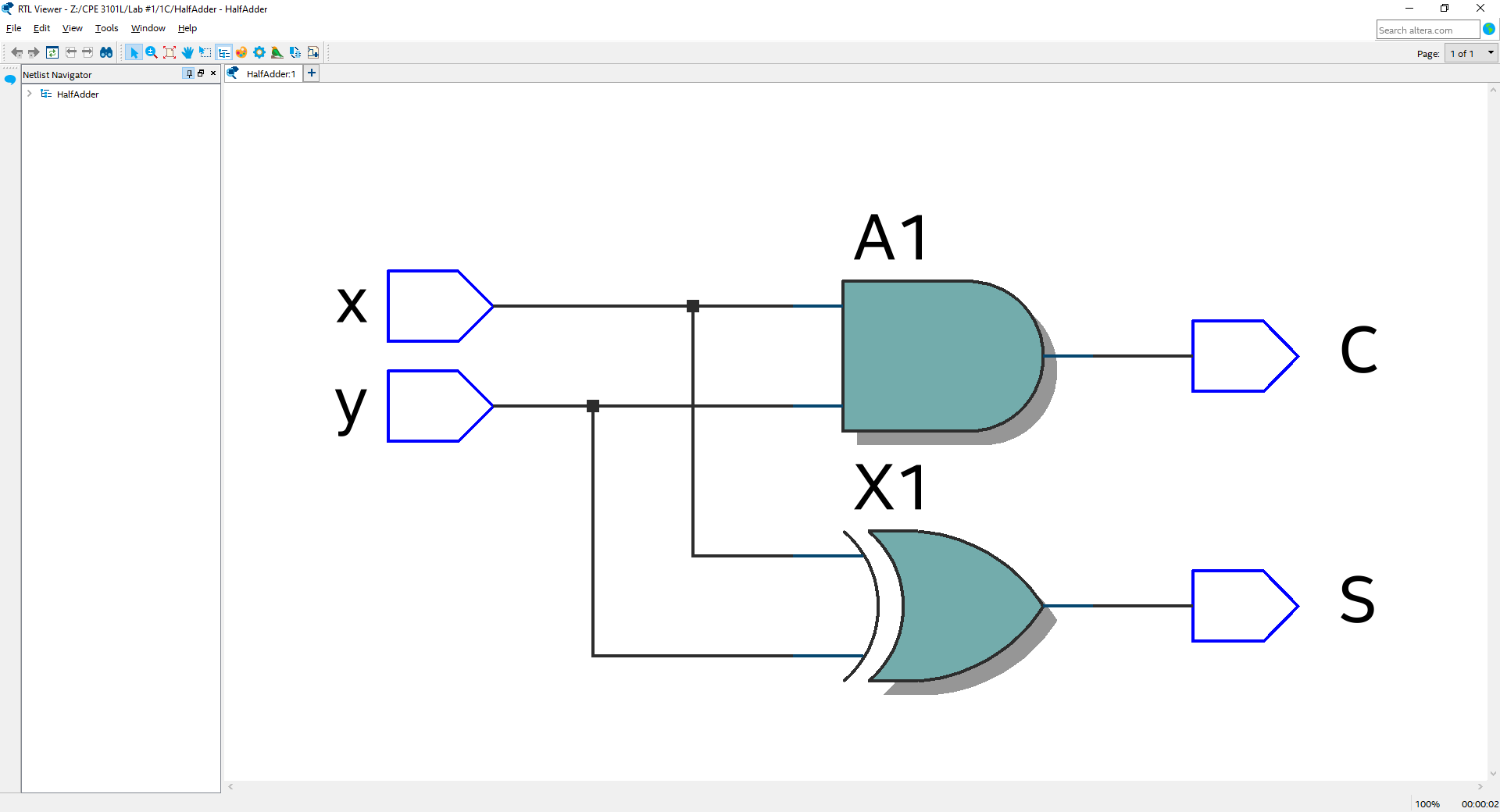
**Figure 2: Design Entry for HalfAdder in Verilog HDL**

As indicated by the code, there will be 2 inputs and 2 outputs, along with the use of 1 XOR and 1 AND gate.



**Figure 3: Compilation Report for the Flow Summary of HalfAdder**

According to the compilation report, 2 logic elements and 4 total pins are needed. Quartus also found 1 warning, however, it is negligible and does not interfere with the synthesis process.



**Figure 4: Schematic Diagram of Synthesized Circuit from HalfAdder Project**

As expected, a half adder circuit was constructed from the design entry. 2 inputs, x and y, are put into both the XOR and AND gates. The result of the AND gate is the CARRY, and the result of the XOR gate is the SUM.